In the Claims

1.-20. (Canceled)

21. (Original) An isolation structure in a semiconductor substrate comprising:

a semiconductor substrate;

a plurality of adjacent trenches in said semiconductor substrate; and

a self-aligned isolation structure in upper portions of selected ones of said plurality of trenches, said isolation structure being merged portions of said semiconductor substrate along at least a first row of said selected ones of said plurality of adjacent trenches, said merged portions of said semiconductor substrate being aligned as-formed to edges of said plurality of adjacent trenches,

wherein said self-aligned isolation structure isolates a first region of said semiconductor substrate from a second region of said semiconductor substrate.

22. (Previously presented) The structure of claim 21 wherein said semiconductor substrate comprises a silicon substrate.

23. (Previously presented) The structure of claim 21 further including a pad dielectric layer thereover a surface of said semiconductor substrate.

24. (Previously presented) The structure of claim 23 wherein said pad dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

25. (Previously presented) The structure of claim 24 wherein said pad oxide layer has a thickness ranging from about 1 nm to about 10 nm.

26. (Previously presented) The structure of claim 24 wherein said pad nitride layer has a thickness ranging from about 50 nm to about 500 nm.

27. (Previously presented) The structure of claim 21 wherein said plurality of adjacent trenches have depths ranging from about 250 nm to about 10μm.

28. (Previously presented) The structure of claim 21 wherein said self-aligned isolation structure comprises a thermal oxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

29. (Previously presented) The structure of claim 28 wherein said semiconductor substrate comprises a silicon substrate and said thermal oxide region comprises a thermal silicon dioxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

30. (Original) An isolation structure in a semiconductor substrate comprising:

a silicon substrate having a layer of pad oxide disposed thereover said silicon substrate and a layer of pad nitride disposed thereover said pad oxide;

a plurality of adjacent trenches traversing through said pad oxide, said pad nitride, and stopping in said silicon substrate; and

a self-aligned, thermal oxide isolation structure in upper portions of said plurality of adjacent trenches, said thermal oxide isolation structure being oxidized portions of said semiconductor substrate merged along at least a first row of selected ones of said plurality of adjacent trenches in said upper portions of said trenches, said oxidized portions of said semiconductor substrate being aligned as-formed to edges of said plurality of adjacent trenches,

wherein said thermal oxide isolation structure isolates a first region of said semiconductor substrate from a second region of said semiconductor substrate.

31. (Currently Amended) An isolation structure in a semiconductor substrate comprising:

a semiconductor substrate;

a plurality of adjacent trenches in said semiconductor substrate having depths ranging from about 250 nm to about 10μm;

a plurality of adjacent segments of said semiconductor substrate between each of said plurality of adjacent trenches;

an oxidation barrier layer residing in lower portions of said plurality of adjacent trenches;

a self-aligned shallow trench isolation comprising merged sections of selected ones of said plurality of adjacent segments of said semiconductor substrate along a first row above said oxidation barrier layer.

32. (Previously presented) The structure of claim 31 wherein said semiconductor substrate comprises a silicon substrate.

33. (Previously presented) The structure of claim 31 further including a pad dielectric layer thereover a surface of said semiconductor substrate.

34. (Previously presented) The structure of claim 33 wherein said pad dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

35. (Previously presented) The structure of claim 31 wherein said oxidation barrier layer is a material selected from the group consisting of local oxidation of silicon, silicon nitride and silicon oxynitride.

36. (Currently Amended) The structure of claim ~~33~~ 31 wherein said oxidation barrier layer has a thickness ranging from about 2nm to about 50nm.

37. (Canceled)

38. (Previously presented) The structure of claim 31 wherein said self-aligned isolation structure comprises a thermal oxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

39. (Previously presented) The structure of claim 38 wherein said semiconductor substrate comprises a silicon substrate and said thermal oxide region comprises a thermal silicon dioxide region existing along said at least first row of selected ones of said plurality of adjacent trenches.

40. (Previously presented) The structure of claim 31 wherein said selected ones of said plurality of adjacent segments of said semiconductor substrate comprise those adjacent segments of said semiconductor substrate along said at least first row having a thinned diameter ranging from about 1/5 to about 1/2 that of a non-thinned, original diameter of said plurality of adjacent segments of said semiconductor substrate.